What is Claimed is:

1. A method of fabricating a MRAM device, comprising:

depositing a first conductive layer on a substrate;

depositing a sense layer on the first conductive layer;

depositing a stop layer on the sense layer;

patterning the stop layer;

etching the stop layer, the sense layer, and the first conductive layer to form a bottom electrode with the sense layer continuous with the bottom electrode in a first direction;

depositing a dielectric layer;

planarizing the dielectric layer;

removing the stop layer to expose a surface of the sense layer;

depositing a plurality of layers of material over the sense layer to form a magnetic tunnel junction stack;

depositing a second conductive layer on a top layer of the plurality of layers of material;

patterning the second conductive layer; and

etching the second conductive layer, the plurality of layers of material, and the sense layer to form a top electrode and a plurality of discrete sense layers,

the plurality of layers of material and the plurality of discrete sense layers define a plurality of discrete magnetic tunnel junction devices, and

the top electrode and the plurality of layers of material are continuous with each other in a second direction.

2. The method as set forth in Claim 1, wherein the planarizing the dielectric layer comprises a chemical mechanical planarization process.

3. The method as set forth in Claim 1, wherein the stop layer comprises a chemical mechanical planarization stop layer.

4. The method as set forth in Claim 3, wherein the planarizing the dielectric layer comprises a chemical mechanical planarization process.

5. The method as set forth in Claim 1, wherein the plurality of layers of material are deposited over the sense layer in a deposition order and the deposition order is determined by a topology for the plurality of magnetic tunnel junction devices.

6. The method as set forth in Claim 1, wherein the etching the stop layer, the sense layer, and the first conductive layer comprises an anisotropic etch process.

7. The method as set forth in Claim 1, wherein the etching the second conductive layer, the plurality of layers of material, and the sense layer comprises an anisotropic etch process.

8. The method as set forth in Claim 1 and further comprising after the etching of the stop layer:

laterally etching the stop layer and the sense layer until the stop layer and the sense layer recede a predetermined distance from an edge of the bottom electrode and the sense layer has a width that is less than a width of the bottom electrode.

9. The method as set forth in Claim 1 and further comprising after the etching of the second conductive layer:

laterally etching the top electrode and the plurality of layers of material until the top electrode and the plurality of layers of material have recessed a predetermined distance from an edge of the discrete sense layer.

10. The method as set forth in Claim 1 and further comprising after the etching of the second conductive layer:

selectively etching the discrete sense layer so that an exposed surface of the discrete sense layer is laterally etched and a length of the discrete sense layer is reduced along the first direction.

11. The method as set forth in Claim 11, wherein the selective etching comprises a wet etch process.

12. The method as set forth in Claim 1 and further comprising:

depositing a dielectric material to fill in a space between the top electrodes and the plurality of layers of material.

13. The method as set forth in Claim 1 and further comprising after the removing the stop layer:

cleaning the surface of the sense layer.

14. A MRAM device fabricated according to the method as set forth in Claim 1.

15. A MRAM device, comprising:

a substrate;

a plurality of bottom electrodes connected with the substrate and substantially aligned with a first direction, the bottom electrodes are separated by a dielectric layer;

a plurality of discrete sense layers connected with the bottom electrodes;

a plurality of top electrodes substantial aligned with a second direction; and

a plurality of layers of material substantially aligned with the second direction and continuous with the top electrodes, a top layer of the plurality of layers of material is in electrical communication with the top electrodes, and a bottom layer of the plurality of layers of material is positioned above the plurality of discrete sense layers and is in electrical communication with the plurality of discrete sense layers, and

wherein the plurality of layers of material and the plurality of discrete sense layers define a plurality of discrete magnetic tunnel junction devices.

16. The MRAM device as set forth in Claim 15, wherein the first direction and the second direction are substantially orthogonal to each other.

17. The MRAM device as set forth in Claim 15, wherein the plurality of layers of material comprises a tunnel barrier layer in contact with the plurality of discrete sense layers and a reference layer in contact with the tunnel barrier layer and the top electrodes.

18. The MRAM device as set forth in Claim 15, wherein the plurality of layers of material comprises a tunnel barrier layer in contact with the plurality of discrete sense layers and a reference layer in contact with the tunnel barrier layer, and a cap layer in contact with the reference layer and the top electrodes.

19. The MRAM device as set forth in Claim 15, wherein the plurality of layers of material comprises a tunnel barrier layer in contact with the plurality of discrete sense layers and a reference layer in contact with the tunnel barrier layer, an anti-ferromagnetic layer in contact with the reference layer, and a cap layer in contact with the anti-ferromagnetic layer and the top electrodes.

20. The MRAM device as set forth in Claim 15, wherein the plurality of discrete magnetic tunnel junction devices are arranged in an array and the top electrode is a selected one of a row conductor or a column conductor and the bottom electrode is a selected one of a row conductor or a column conductor.

21. The MRAM device as set forth in Claim 15, wherein an area of the plurality of discrete magnetic tunnel junction devices is determined by a width of the top electrode and a width of the bottom electrode.

22. The MRAM device as set forth in Claim 15, wherein the plurality of layers of material are defined by a topology for the plurality of magnetic tunnel junction devices.

23. A method of fabricating a MRAM device, comprising:

depositing a first conductive layer on a substrate;

depositing a sense layer on the first conductive layer;

patterning the sense layer;

etching the sense layer and the first conductive layer to form a bottom electrode with the sense layer continuous with the bottom electrode in a first direction;

depositing a dielectric layer;

planarizing the dielectric layer;

depositing a plurality of layers of material over the sense layer to form a magnetic tunnel junction stack;

depositing a second conductive layer on a top layer of the plurality of layers of material;

patterning the second conductive layer; and

etching the second conductive layer, the plurality of layers of material, and the sense layer to form a top electrode and a plurality of discrete sense layers, the top electrode and the plurality of layers of material are continuous with each other in a second direction, and

the plurality of layers of material and the plurality of discrete sense layers define a plurality of discrete magnetic tunnel junction devices.

24. The method as set forth in Claim 23, wherein the planarizing the dielectric layer comprises a chemical mechanical planarization process.

25. The method as set forth in Claim 23, wherein the plurality of layers of material are deposited over the sense layer in a deposition order and the deposition order is determined by a topology for the plurality of magnetic tunnel junction devices.

26. The method as set forth in Claim 23 and further comprising:

depositing a dielectric material to fill in a space between the top electrodes and the plurality of layers of material.

27. The method as set forth in Claim 23 and further comprising after the planarizing the dielectric layer:

cleaning the surface of the sense layer.

28. A MRAM device fabricated according to the method as set forth in Claim 23.